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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,790	01/15/2004	Thomas Joseph Beacom	ROC920030257US1	5443

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EXAMINER

CONTINO, PAUL F

ART UNIT	PAPER NUMBER
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2114

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/757,790

Applicant(s)

BEACOM ET AL.

Examiner

Paul Contino

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 14-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION: Non-Final Rejection**

*Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
  - I. Claims 1-13, drawn to processor diagnostics, classified in class 714, subclass 37.
  - II. Claims 14-20, drawn to error detection, classified in class 714, subclass 48.
2. The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and Group II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different designs, modes of operation, and effects (MPEP § 802.01 and § 806.06). In the instant case, the different inventions are directed to processor diagnostics and error detection, respectively.

Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.
3. During a telephone conversation with Robert R. Williams (Reg. No. 48,395) on August 15, 2006, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-13. Affirmation of this election must be made by applicant in replying to this Office action. Claims 14-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

*Specification*

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: ERROR DETECTION DURING PROCESSOR IDLE CYCLES.

*Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 4 and 10-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As in claim 4, the claimed “pre-computed result” is used in a different context from that as disclosed throughout the Specification (see Figure 2 #280 and page 12 lines 17-20 and page 13 lines 17-20, pre-computed result 280, as examples). The Specification uses a “pre-computed result” as a single value to compare the result of multiple computations via diagnostic instructions. The claim uses this term as multiple intermediary results between instructions. Because of these two distinct definitions relating to a single term, the Examiner recommends the

language “pre-computed result” as used in claim 4 be amended in order to overcome the lack of enablement rejection.

As in claim 10, in lines 16-18 of page 19, the description above pertaining to claim 4 is applied. An antecedent basis problem arises in line 19, where “the pre-computed result” should be changed to “a pre-computed result”. Lines 19-20 describes comparing a result of “each of the diagnostic instructions” with the “pre-computed result” which is also not disclosed in the disclosure of the Specification. The only comparison found in the Specification is a single comparison between the final result of the diagnostic instructions and a single pre-computer result. Claims 11-13 are rejected based upon their dependence to claim 10.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Vea (U.S. Patent No. 4,924,428).

As in claim 1, Vea discloses a method comprising:

detecting an event that would cause cycles to be idle in a processor (*column 3 lines 4-10, where it is inherent that a event be detected in order to cause processor idle cycles*); and

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issuing diagnostic instructions to the processor during the cycles that would be idle  
(column 3 lines 4-10).

\* \* \*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Vorbach et al. (U.S. Patent No. 6,697,979).

As in claim 1, Vorbach et al. discloses a method comprising:

detecting an event that would cause cycles to be idle in a processor (column 4 line 65 through column 5 line 10, and column 10 lines 49-53, where it is inherent that a event be detected in order to cause a processor IDLE cycle); and

issuing diagnostic instructions to the processor during the cycles that would be idle (column 4 line 65 through column 5 line 10).

As in claim 2, Vorbach et al. discloses selecting the diagnostic instructions based on a number of the cycles that would be idle (column 5 lines 7-10).

As in claim 3, Vorbach et al. discloses comparing a result of the diagnostic instructions with a pre-computed result (*column 3 lines 48-54, where it is interpreted that the setpoint result is pre-computed*).

As in claim 6, Vorbach et al. discloses the event comprises a task switch (*column 5 lines 1-2, where the switching from a program task running on a computer to no program running implies a task switch causing idle processor cycles*).

As in claim 7, Vorbach et al. discloses an apparatus comprising:

means for detecting an event that would cause cycles to be idle in a processor (*column 4 line 65 through column 5 line 10, and column 10 lines 49-53, where it is inherent that a event be detected in order to cause a processor IDLE cycle*);

means for issuing diagnostic instructions to the processor during the cycles that would be idle (*column 4 line 65 through column 5 line 10*); and

means for comparing a result of the diagnostic instructions with a pre-computed result (*column 3 lines 48-54, where it is interpreted that the setpoint result is pre-computed*).

As in claim 8, Vorbach et al. discloses means for selecting the diagnostic instructions based on a number of the cycles that would be idle (*column 5 lines 7-10*).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Veal in the invention of Zilka (U.S. PGPub 2003/0061383).

As in claim 5, Veal teaches of an event causing a processor to idle. However, Veal fails to teach of processor idling in response to a cache miss. Zilka teaches of a processor idling in response to a cache miss (*paragraph [0012]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the cache miss event response as taught by Zilka in the invention of Veal. This would have been obvious because the invention of Zilka reduces the power consumption necessary to operate a computer system (*paragraph [0003]*).

\* \* \*

9. Claims 4, 9, 10, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vorbach in view of Kromer (U.S. PGPub 2004/0255099).



As in claims 4 and 9, Vorbach teaches the limitations of claims 1 and 7, respectively. However, Vorbach fails to teach of result of a previous instruction being input to an immediate subsequent instruction. Kromer teaches of incrementing a pre-computed result between the diagnostic instructions wherein the pre-computed result of one of the diagnostic instructions is input to a next of the diagnostic instructions (*paragraphs [0032]-[0040], where the term "incrementing" as read in light of the Applicant's Specification on page 13 in lines 21-23 is interpreted as any type of instruction operation carried out on the result*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the using of results as input as taught by Kromer in the invention of Vorbach. This would have been obvious because the invention of Kromer reduces the amount of circuitry needed to carry out processing, which reduces the cost and increases the efficiency of such a computer system (*paragraph 0014*). Further, it is well known in the art to have an instruction compute a value and then use that computed value in a next instruction, regardless of the application. The claimed invention as interpreted by the Examiner relates only to instructions that are placed one after the other in this manner in a diagnostic system, which is not interpreted as being novel over the applied prior art.

As in claim 10, Vorbach teaches a processor comprising:

an issue unit to detect an event that would cause cycles to be idle in the processor and issue diagnostic instructions during the cycles that would be idle to a pipeline (*column 4 line 65 through column 5 line 10, and column 10 lines 49-53, where it is inherent that a event be detected in order to cause a processor IDLE cycle*); and

a compare unit to compare the pre-computed result with a [final] result of [[each of]] the diagnostic instructions (*column 3 lines 48-54, where it is interpreted that the setpoint result is pre-computed*).

However, Vorbach fails to teach of result of a previous instruction being input to an immediate subsequent instruction. Kromer teaches of an increment unit to increment a pre-computed result between the diagnostic instructions wherein the pre-computed result of one of the diagnostic instructions is input to a next of the diagnostic instructions (*paragraphs [0032]-[0040]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the using of results as input as taught by Kromer in the invention of Vorbach. This would have been obvious because the invention of Kromer reduces the amount of circuitry needed to carry out processing, which reduces the cost and increases the efficiency of such a computer system (*paragraph 0014*).

As in claim 11, Vorbach teaches the issue unit is further to select the diagnostic instructions based on a number of the cycles (*column 5 lines 7-10*).

As in claim 13, Vorbach teaches the event comprises a task switch (*column 5 lines 1-2, where the switching from a program task running on a computer to no program running implies a task switch causing idle processor cycles*).

\* \* \*

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vorbach in view of Kromer, further in view of Zilka.

As in claim 12, the combined invention of Vorbach and Kromer teaches of an event causing a processor to idle. However, the combined invention of Vorbach and Kromer fails to teach of processor idling in response to a cache miss. Zilka teaches of a processor idling in response to a cache miss (*paragraph [0012]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the cache miss event response as taught by Zilka in the combined invention of Vorbach and Kromer. This would have been obvious because the invention of Zilka reduces the power consumption necessary to operate a computer system (*paragraph [0003]*).

### *Conclusion*

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC  
8/19/2006



**SCOTT BADERMAN**  
**SUPERVISORY PATENT EXAMINER**